Internship Report

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Abstract: In the first part of this report considerations about the emulation circuitry for the AdEx model done in [3] are made and analytical analysis for ideal and numerical considerations non-ideal circuit behaviour are presented. The second part consists of simulations done on the emulation circuit for the AdEx neuron. The testbench used for these simulations is described and a number of states found in literature are reproduced.

Contents

1 Introduction

The part of the Human Brain Project [1] project I was working on in this internship aims at building a waferscale neuromorphic device capable of emulating the adaptive integrate and fire neuron model (short: AdEx) [4]. The development of the integration is described in [1] and [3]. The aim of this waferscale integration is to enable neuromorphic experiments on a scale not accessible with conventional simulation in concerns of speed and power efficiency. A neuron model was designed and tested by Sebastian Millner in the thesis cited above. This work is about further testing the capability and limitations of the neuron model. First an analytical analysis is done, assuming ideal circuit elements. This analysis is used to get equations for parameter translations in numerical treatment of simulation results of the transistor level circuits. The derived equations are inverted to be able to calculate the parameters needed for certain time constants. In the second part of this internship report the response of the circuit to variation of a number of parameters is recorded in transistor level simulations using a neuron testbench that is described in the appendix. Also some spiking patterns found in literature are shown and discussed.

2 Theory

2.1 AdEx model equations

As they are referenced heavily in this report I describe the fundamentals of the AdEx model [4]. I rely on the description given in [3] as well.

The two dimensional model describes the activity of a neuron and is based on an integrate and fire neuron model. As a description for the state of the neuron the voltage over the membrane (V) is chosen.

$$-C_m\frac{dV}{dt} = g_l(V-E_l) - g_l\Delta_t e^{\frac{V-V_t}{\Delta_t}} + g_e(t)(V-E_e) + g_i(t)(V-E_i) + w \quad (1)$$

$$-\tau_w\frac{dw}{dt} = w - a(V-E_l) \quad (2)$$

Here g_L, $g_e(t)$ and $g_i(t)$ are the conductances for leakage, excitatory and inhibitory synapses, just as E_l, E_e and E_i are the reversal potentials for the respective terms. C_m, Δ_t and V_t are the membrane capacitance, the slope factor and the spike threshold. Finally w is the adaptation current, τ_w the adaptation time constant and a the subthreshold adaptation conductance.

When the membrane voltage reaches a certain threshold Θ a spike is fired. In the model this means the membrane voltage is set to a reset value and the adaptation current is increased by b to implement spike triggered adaptation.

[1] Human Brain Project, website of subdivision: https://www.humanbrainproject.eu/de/neuromorphic-computing-platform

$$V \to V_{\text{reset}} \tag{3}$$

$$w \to w + b \tag{4}$$

These differential equations are emulated in a circuit designed in [3], containing a transformation of the adaptation current w found in section 3.5.1 of the cited dissertation:

$$w = a(V_w - E_l) \tag{5}$$

Here V_w is called adaptation voltage. Whit this transformation the literature equations can be rewritten in a way that allows for better translation into circuits:

$$-C_m \frac{dV}{dt} = g_l(V-E_l) - g_l \Delta_t e^{\frac{V-V_t}{\Delta_t}} + g_e(V-E_e) + g_i(V-E_i) + a(V_w-E_l) - I \tag{6}$$

$$-C_w \frac{dV_w}{dt} = g_w(V_w - V) \tag{7}$$

The reset condition has to be rewritten as well, to accommodate the fact that the measure of adaptation is a voltage now and not a current:

$$V_w \to V_w + V_q \tag{8}$$

Here V_q is the voltage rise of the adaptation voltage at spike time. In the rest of the document (6), (7) and (8) are used as representation of the AdEx equations.

2.2 Simulation results found in literature

A part of this report will concentrate on reproducing certain spiking patterns that can be found in literature and are basic requirements of any neuron model. In [2] the biological relevance of the various spiking patterns is discussed. Included in that paper is also a overview over the transient behaviour for these states summarized in a plot taken from that paper (figure 1).

Directly liked to our experiment is [6]. Here the focus is on spiking pattern reproducible with the AdEx neuron model. This publication allows for the comparison of phase plane trajectories as well. Some of the spiking patterns shown there can be reproduced in our circuit.

3 Translation of the AdEx parameters

The neuron emulation discussed here was developed in [3]. It realizes the terms of the AdEx model as separate circuits, as shown in (figure 2). The neuron model is tuned by a large quantity of parameters, all of which are accessible to the neuron testing environment. A description of this environment is given in

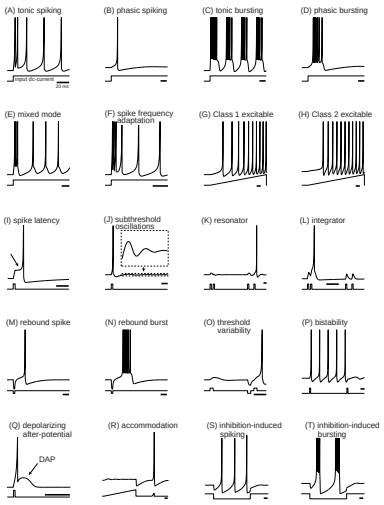


Figure 1: This picture summarizes the neuro-computational properties of biological neurons. Electronic version of the figure and reproduction permissions are freely available at www.izhikevich.com

the appendix, containing all parameters that can be tuned on the testbench and describing each pin and its function available on the circuits representation the terms of the AdEx model in detail.

3.1 Analytical treatment assuming ideal circuit elements

This section summarises work done in [3] and aided by Andreas Hartel, who contributed the analytical treatment of the exponential term. The synaptic terms will be neglected in this analysis, as they are not central to the neuron models behaviour and would need further analysis.

The conductances in the circuit are realized as Operational Transconductance Amplifiers (short: OTA). A ideal OTA is characterized by the following equation [7]:

$$I_{out} = h \cdot I_{bias}(V_+ - V_-) \tag{9}$$

Here I_{out} is the output current, I_{bias} the biascurrent and V_+, V_- are the voltages at the negative and positive input of the OTA. h is a parameter containing dependency on process, circuit and temperature. This ideal OTA can be set to any conductance value by adjusting the current I_{bias}.

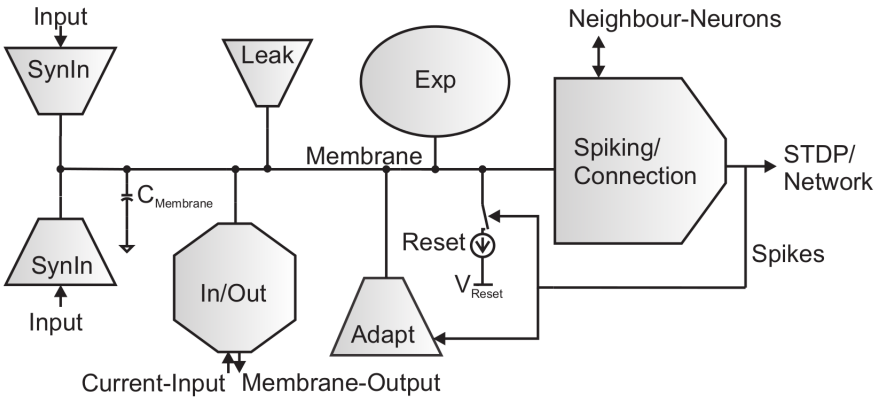


Figure 2: Overview over the simplified neuron schematics. The various parameters affection the subcircuits are explained in the appendix. Picture taken from [1]

All terms of the form "current = conductance (voltage1 - voltage2)" are realized as OTAs in the emulation circuit.

The only term containing a different structure is the exponential term, whose ideal circuit behaviour can be described by the following equation provided by Andreas Hartel, that finalizes analysis made in [3]:

$$I_{exp} = I_0 exp\left(\frac{V_{mem} - V_{exp} - 5R_2 I_{rexp}}{4\lambda n U_T R_2 I_{rexp}} - \frac{U_{th}}{nU_T}\right) \tag{10}$$

Matched with the term given in the theoretical model ($g_l \Delta_t e^{\frac{V-V_t}{\Delta_t}}$) this gives for the slope factor (Δ_t) and the product of slope factor and leakage conductance ($g_l \Delta_t$):

$$\Delta_t = 4\lambda n U_T R_2 I_{rexp}$$

$$"g_l \Delta_t" = I_0 exp\left(-\frac{5}{4\lambda n U_T} - \frac{U_{th}}{nU_T}\right)$$

Important to mention here is that the term representing the fore factor is not identical to the product of I_{gl} and Δ_t. This is a imperfection of the circuit, even when considering perfect circuit elements.

Excluding the synaptic terms we can now give a representation of the AdEx equations, containing only hardware parameters. The validity of these equations is very limited, as the circuit elements do not behave ideally, but this can be used as basis for the numerical treatment of simulation results in the next section.

$$-C_m\frac{dV}{dt} = h_{gl}I_{gl}(V-E_l) - I_0 exp\left(\frac{V-V_{exp}-5R_2I_{rexp}}{4\lambda nU_T R_2 I_{rexp}} - \frac{U_{th}}{nU_t}\right) + h_{adaptgl}I_{gladapt}(V_w - E_l) - I \tag{11}$$

$$-C_w\frac{dV_w}{dt} = h_{radapt}I_{radapt}(V_w - V) \tag{12}$$

The additional voltage that adds to the adaptation voltage is realized by a defined charge flowing on the capacitor storing that voltage:

$$V_w \to V_w + \frac{t_{fire}I_{fireb}}{C_w} \tag{13}$$

The reset functionality for the membrane potential can still be modelled by 3.

3.2 Numerical treatment of transistor level circuits

The equations given above would be sufficient for describing the circuit, if the circuit elements (like OTAs and amplifiers) would act like ideal models. As this is not the case the derivations from the ideal behaviour need to be taken into account.

The terms in the above equations are using just two kinds of devices: The OTA and the exponential circuit. Both will need to be analysed to get a correct translation of the hardware parameters to the circuits behaviour.

The OTA is sensitive to voltage differences and the range in which the output current depends linearly on the voltage difference at the input terminals is limited as found in [3]. Here I redid some of the plots found there to get the functional dependence of the conductance on the biascurrent I_{bias}.

The OTA is set up like in the leakage term, the voltage at the positive terminal is fixed, the voltage at the negative terminal is sweeped over the valid range (0 to 1.8 V). The output current and the sweeped voltage are recorded and exported to a pyhton script. From this data the conductance is derived (derivative of the I-U-curve). The derived data is averaged over a range of ± 150 mV, a procedure similar to [3, Figure 3.9]. This averaged value is recorded for all bias currents. A polynomial of the 3. Order is fitted to the dependence of the averaged conductance vs. the bias current.

$$f(x) = ax^3 + bx^2 + cx + d \tag{14}$$

This is done for various voltage levels, to verify that the OTA behaviour does not depend to heavily on this and see possible differences from ideal behaviour. To get an overview over the results see figure 3.

Quite large deviations from the ideal behaviour can be found, the OTA is not scaling linearly over the whole voltage range. The behaviour is rather

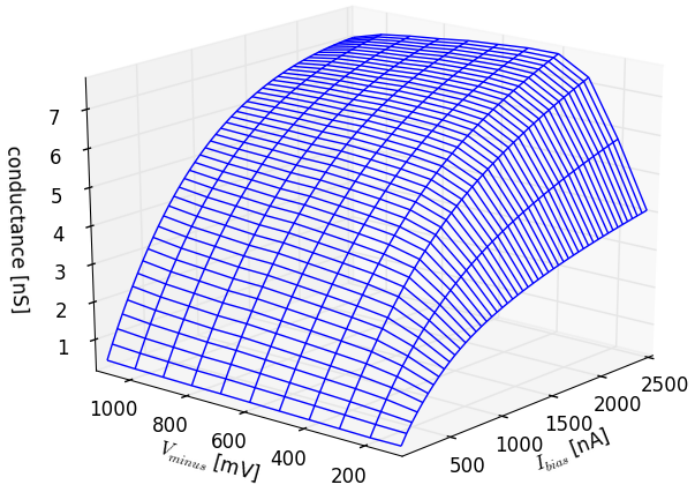


Figure 3: plot showing the conductance against the bias current I_{bias} and the voltage at the negative input that is hold fastened. The conductance was calculated using scans of the negative terminal, plotting the output current onto the voltage supply that was connected to the negative output vs the voltage difference between the two terminals. The derivative of this curve was averaged over ± 150 mV. Each point in this plot is such a mean value of derivatives.

cubic. While this is hardly noticeable as long as one stays within range of the bias current it becomes apparent in the used variety of different voltage ranges that can be found in the experiment.

As visible in 3 the conductance is almost independent of the membrane voltage in a range from about 400mV to 1000mV. I averaged the fit parameters over this range and derived one equation catering for this range with good precision.

$$\begin{aligned} a &= (3.30 \pm 0.22)10^{-10} \\ b &= (-2.53 \pm 0.12)10^{-6} \\ c &= (7.41 \pm 0.15)10^{-3} \\ d &= (3.419 \pm 0.030)10^{-1} \end{aligned} \tag{15}$$

To get a full understanding of the circuits and to be able to plot the nullcline, a similar analysis of the exponential term would be needed. This is omitted,

voltage [mV]	a [10^{-10}]	b [10^{-6}]	c [10^{-3}]	d [10^{-1}]
100	3.9119	- 2.1652	4.6016	0.029912
200	3.7851	-2.3214	5.8151	- 1.8854
300	3.3932	- 2.3354	6.7215	-3.3866
400	2.6665	- 2.1177	6.8133	-3.4949
500	2.7289	-2.2170	7.0302	-3.4447
600	2.9114	-2.3456	7.2174	- 3.4417
700	3.1960	- 2.5062	7.4203	- 3.4504
800	3.5020	-2.6676	7.6087	- 3.4407
900	3.7987	- 2.8230	7.7789	- 3.4301
1000	4.2792	- 3.0548	8.0220	-3.2431
1100	4.3936	- 3.1610	8.1063	- 3.2777
1200	5.8262	- 3.8404	8.4810	- 3.3919

Table 1: Fitparameters for different fixed voltages at the positive terminal are scanned. Used in a polynomial $f(I_{bias}) = aI_{bias}^3 + bI_{bias}^2 + cI_{bias}$ they translate the bias current into the OTA's conductance. These conductances where averaged over a ± 150 mV interval, outside this interval the equations start to deviate a lot from the actual measurement (due to saturation effects).

because of timing reasons. In [3] additional details about this circuit can be found

4 Spiking behaviour in transitor-level simulations

This chapter aims at gaining further insight into the system by simulation of the complete circuit with transistor level simulations. This is important, as the analytical and numerical considerations above do not take all parameters into account, as the parameter space is to big to derive useful spaces changing all parameters. As these transistor level simulations of the whole circuit take quite long (approximately 5 to 20 minutes per analysis), a multi dimensional sweep over all available parameters (ca. 20) using 100 points in each parameter sweep in the valid ranges to cover everything would take significantly longer than the universe is old. Therefore I chose to do the sweeps one dimensional for a limited number of interesting neural states in the first section of this chapter.

While doing these analysis I wrote a documentation about the neuron testing environment to be able to understand what I can influence in the circuit. Many of the parameters have technical meaning and do not have to be altered, I concentrated the sweeps on parameters that have direct relation to the AdEx model and left the others untouched.

In the first section the above described sweeps are performed, and the reaction of the circuit recorded. The second section focuses on reproducing states found in literature.

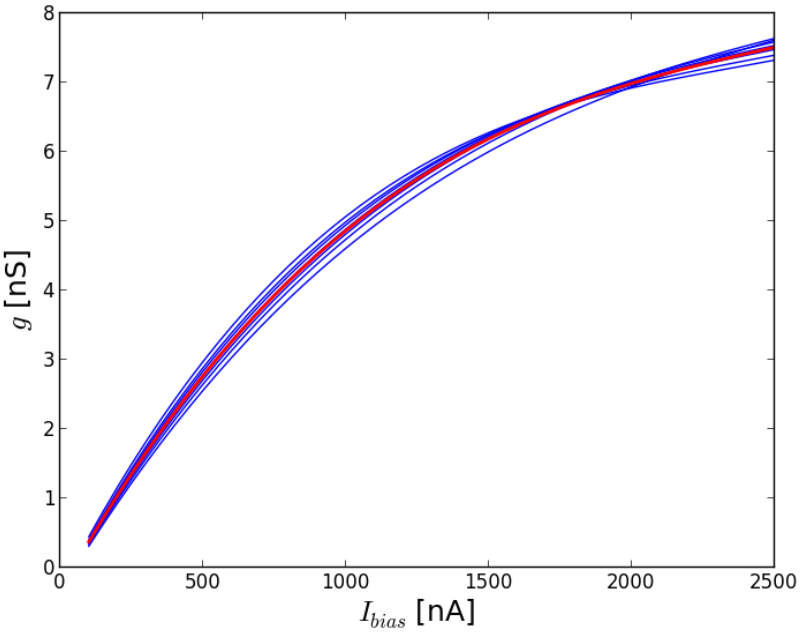


Figure 4: This shows the mean fit for the plateau. In blue all fits in the range between 400mV to 1000mV are shown. In red the curve that is made up of the mean fits is plotted.

4.1 Sweeping parameters for basic patterns

In this section the parameter sweeps described above will be done on three basic patterns: "tonic spiking", "adaptation" and "tonic bursting". The state of toinc bursting contains initial bursting as a special case. In all these simulations a current step of 600 nA amplitude and 16 μs is used to stimulate the neuron. The total simulation length is always chosen to be 35 μs (16 μs before and 3 μs after the stimulation are visible). The parametrization given in 2 is used for each analysis. This parametrisation is only altered in the variable described and the influence of that variable on the circuit is recorded.

4.1.1 Tonic Spiking Neuron

Tonic Spiking describes the reaction of a type of neuron that reacts to step-current-stimulation by repetitive spiking with constant frequency. This is a spiking pattern that can be realized without complications on the AdEx emulation circuit. To reach this pattern the adaptation is turned off. This can be easily achieved by setting the bias current for the Output of the adaptation OTA to 0 (I_{gladapt}). Further explanations concerning this state can be found in

section 4.2.

In the following list an overview over the change that the system is experiencing is given due to changes in certain parameters. This should give an overview over the behaviour on the neuron emulation circuit in total.

- E_l: When E_l is chosen very low (more than 60mV below the exponential threshold), no spiking behaviour is visible, as the leakage current draws the membrane down to the leakage potential. With increasing E_l the neuron starts spiking with increasing frequency. If E_l is chosen very high (voltage similar to exponential threshold), the neuron fires spikes even without stimulation.

- V_exp: When V_exp is chosen very low (about 100mV below E_l), the neuron spikes continuous, as the threshold for the exponential rise is depended on this voltage (section: 3.2). When V_exp is chosen higher, the spiking threshold rises and fewer spikes are emitted. When V_exp is to high the spiking threshold is not reached and no spikes are emitted.

- V_t: When V_t is below V_reset and E_l there is a continuous reset and the neuron does not start spiking, but stays on the reset potential. When V_t is growing, there is a steeper part of the exponential term showing, when its very high saturation effects start to play a role and inhibit further rise.

- I_bexpb: for very low values of I_bexpb the exponential rise is very broad, with rising values it gets narrow. The spike frequency rises analog to this development.

- I_gl: has almost no effect on the spiking behaviour, only a small rise in the spiking frequency can be observed, as the value for I_gl grows.

- I_rexp: For very low values of I_rexp (0n to 240nA) we get very high frequency spiking, with and without stimulus. Next to this regime a higher value of I_rexp means a higher threshold voltage. As soon as the threshold voltage is not reached any more by the excitation, no spiking is observed.

4.1.2 Spike Frequency Adaptation

Spike frequency adaptation is basically tonic spiking with decreasing frequency [2]. The answers of this spiking pattern to most of the parameters described above is similar to tonic spiking, but certain parameters that where turned off before effect the behaviour now, for the other parameter see section 4.1.1.

- I_fire: With rising I_fire (named I_adaptb on the testbench) the current that is flowing on the adaptation capacitor grows and the adaptation voltage rises. That means a higher I_fire results in greater adaptation per spike.

- I_gladapt: Small values mean that next to no current is put out by the adaptation OTA, so no adaptation can be observed.

- I_{radapt}: This current controls the amount of discharge that happens in the subthreshold regime.

4.1.3 Tonic Bursting

Following [6] we define a burst as a number of sharp resets followed by a broad reset. The room in the parameter space for this firing pattern is very small, only for certain differences of the reset voltage and the exponential threshold we get bursting behaviour. Further explanations can be found in section 4.2.

- E_l: If the leakage potential E_l is very low the membrane voltage is to low to ever reach V_T. By choosing E_l larger more bursts and more spikes per burst can be observed. If E_l is chosen too high the neuron fires continuously.
- I_{bexpb}: The offset current of the operational amplifier regulates the strength of the exponential rise as soon as V_T is reached, higher values result in a steeper rise.
- I_{fire}: Low values of I_{fire} result in many spikes per burst, high values decrease it so much that the system crosses the V-nullcline with one spike, resulting in slow tonic spiking.
- I_{gl}: A rising leakage current draws the system faster back to leakage and lowers the V-nullcline. This results in a decrease of spikes per burst with increasing I_{gl}.
- $I_{gladapt}$: The influence of the adaptation current grows with this quantity, higher values result in lower frequency. System transversing from tonic spiking to bursting with lowering spiking frequency.
- I_{pl}: for low values of I_{pl} slow tonic spiking can be observed. For higher values this transverses via a regime where bursting is possible into continuous spiking with very high frequency.
- I_{radapt}: With higher bias current for the subthreshold adaptation the recovery of the adaptation Voltage (and therefore the adaptation current) decline faster, resulting in higher bursting frequency.
- V_t: if the spike threshold is below E_l and V_{reset} the membrane voltage is continuously reset. At higher values the number of spikes per burst grows with V_t.
- I_{rexp}: For very low values of I_{rexp} the exponential threshold is very low, resulting in high spiking frequency (permanent spiking if V_t is low enough). For too high values the threshold can not be reached any more. The tonic bursting regime is just a few nA wide and surrounded by tonic spiking for lower values and initial bursting [6] (also called mixed mode [2]) for higher values.

- $I_{spikeamp}$: As the offset voltage for the comparator gets higher, the frequency of spiking (for higher values bursting) grows. The voltage at which a spike is detected is lower for higher voltages.

- V_{exp}: For very low values the exponential threshold is reached continuously, for high values the spiking threshold is not reached any more. In the intermediate regime there is a small voltage range for tonic bursting, surrounded by tonic spiking on the lower side and initial bursting on the other.

- V_t: For very low values (below E_l, V_{reset}) we get continuous reset like before. When the reset voltage is high, there are more spikes per burst. If the value is to high (more than 350 mV above E_l) there is no reset any more

- V_{reset}: Bursting is, as pointed out in [3], extremely sensitive to variation in the reset voltage, as this voltage determines the line of constant membrane voltage where the system climbs up the the V-nullcline. In the presented setting tonic bursting is just visible for a single mV step.

quantity	tonic spiking	spike frequency adaptation	tonic bursting
E_{l}	880 mV	880 mV	860 mV
E_{syni}	800 mV	800 mV	800 mV
E_{synx}	1.4 V	1.4 V	1.4 V
I_{bexpb}	2 uA	2 uA	2 uA
I_{convi}	0	0	0
I_{convx}	0	0	0
I_{adaptb}	100 nA	100n	1u
I_{gl}	1.8 uA	1.8 uA	900 nA
I_{gladapt}	0	900 nA	900 nA
I_{intbb}	1 uA	1 uA	1 uA
I_{pulse}	500 nA	500 nA	500n
I_{radapt}	500 nA	500 nA	2u
I_{rexp}	400 nA	400 nA	195 nA
I_{spikeamp}	1 uA	1 uA	1 uA
V_{exp}	820mV	820 mV	820 mV
V_{syni}	1V	1 V	1 V
V_{syntci}	1.4 V	1.4 V	1.4 V
V_{syntcx}	1.4 V	1.4 V	1.4 V
V_{synx}	1 V	1 V	1 V
V_{t}	1.1 V	1.1 V	1.1 V
V_{reset}	850 mV	850 mV	857 mV

Table 2

4.2 Reproduction of neuron states found in literature

First I will try to reproduce the firing states found in [6] shown here in a figure taken out of that paper (figure 5). The ability to produce these diagrams is central for the emulating circuit, as it shows its ability to cater for different neuron types that are found in the cortex. As an important reference for this [2] is used, as it includes links between the spiking patterns and biological neurons.

In the following sections the various spiking patterns that could be reproduced are discussed and the link to simulation literature pointed out.

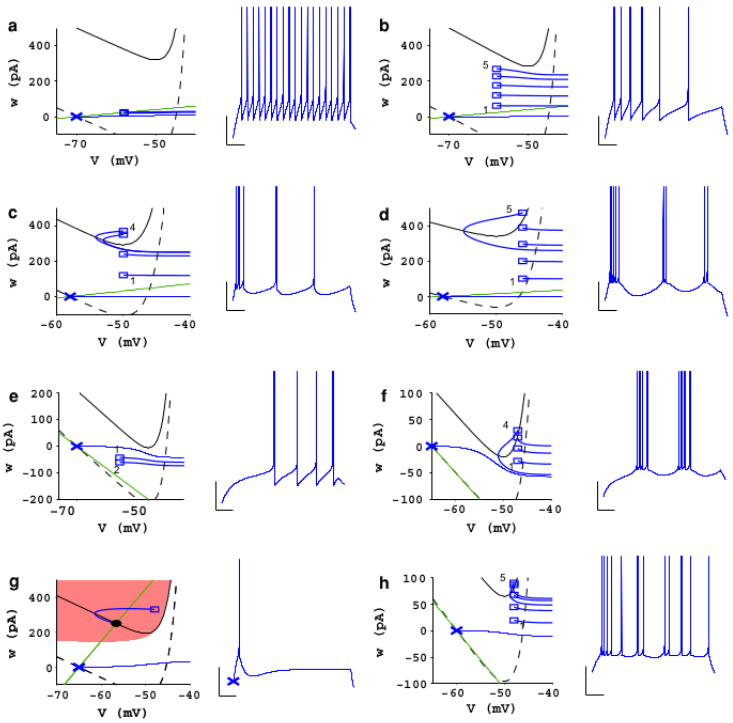
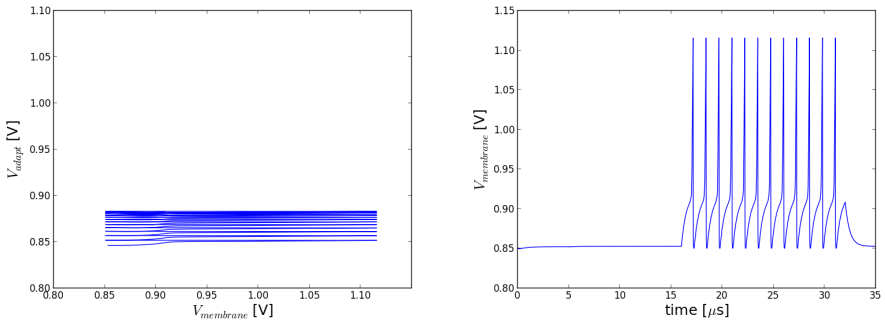


Figure 5: "Phase plane representation of eight firing patterns. Firing patterns observed during a step current stimulation are: **a** tonic spiking, **b** adaptation, **c** initial burst, **d** regular bursting, **e** delayed accelerating, **f** delayed regular bursting, **g** transient spiking and **h** irregular spiking." Figure and caption taken from [6]

4.2.1 Tonic Spiking

Tonic spiking neurons fire spikes with constant frequency when stimulated. There is no alteration of the spiking frequency visible. In our model this is done by turning the adaptation current of by setting $I_{gladapt}$ to 0 and inhibiting the accumulation of adaptation voltage by turning off the I_{fire} current that

charges the membrane (just like descibed before). The result of this is visible in 6. There is still some accumulation of adaptation voltage visible in the phase-diagram, but it is one order of magnitude smaller than for the other spiking states. This state resembles a out of 5. It can be found in 1 as subfigure (A).

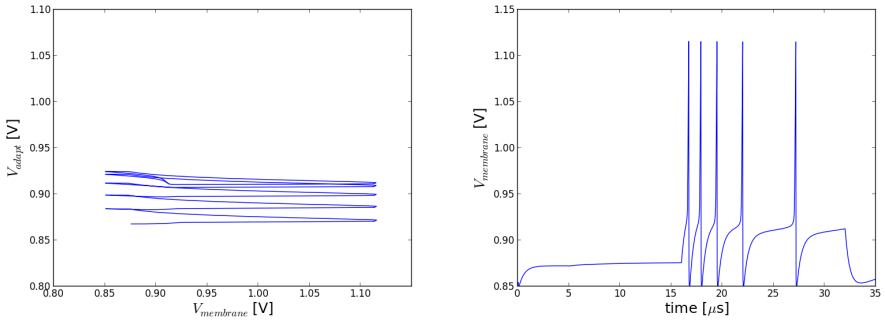


(a) (b)

Figure 6: Tonic spiking observed in the transistor-level simulation of the neuron model. This pattern is similar to the tonic spiking state found in figure 5

4.2.2 Adaptation

The adaptation state is very much similar to the tonic spiking state, with the change that here the accumulation of adaptation voltage is turned on (via I_{fire}) and the adaptation current is turned on ($I_{gladapt}$). Clearly visible is the decrease of spiking frequency with every spike like in subfigure b out of figure 5 or in figure 1 as subfigure (F).

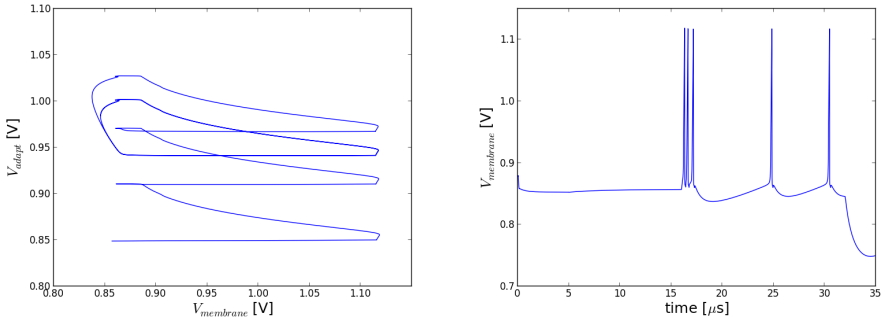


(a) (b)

Figure 7: Adapation

4.2.3 Inital Burst

The inital burst state in [6] can be found in 1 as subfigure (E) under the name mixed mode. It is obtained in the simulation by enhancing a tonic bursting state by rising the I_{radapt} current, so that once the system crosses the nullcline, it transverses that point with every spike following again. This results in low frequency spiking behaviour.

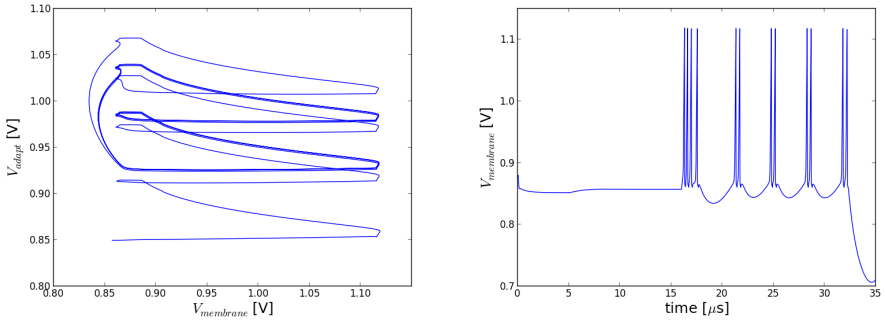


(a) (b)

Figure 8: Inital Burst, also called mixed mode in [2]

4.2.4 Regular Bursting

The regular bursting state out of [6], also called tonic bursting in 1 is possible only for a very small room in parameter space. Especially for V_{reset} the range of voltages for that this behaviour is observed is very small (see discussion in [3] and above). According to [2] these states are believed to contribute to gamma oscillations in the brain.

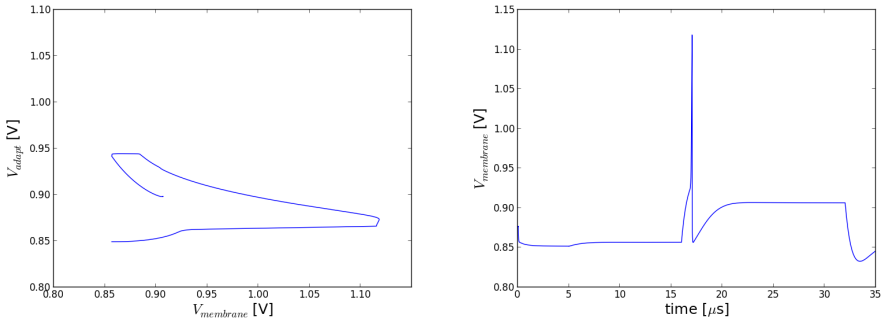


(a) (b)

Figure 9: Regular Bursting, also called tonic bursting in [2]

4.2.5 Transient Spiking

In this state, which is called phasic spiking in 1 one can observe only one spike at the onset of the stimulus and no other state following. Behaviour like this is obtained by making the amount of adaptation per spike quite large and slowly decaying (in hardware parameters this means hight I_{fire} and low I_{radapt}), connected whit a high threshold for spiking (in hardware: high value for V_{exp}) that is not reached when any adaptation current is flowing.



(a) (b)

Figure 10: Transient Spiking, also called phasic spike in [2]

5 Conclusion and Outlook

This internship consisted totally of work on the 180nm HICANN neuron. I summarized findings out of [3] assuming ideal behaviour for all elements. I had a close look on what the characteristics of the OTA[2] are and how to describe the bias current I_{bias} changes the conductance behaviour. Also I wrote a documentation about the various variables I encountered during my work with the neuron testbench. I showed how the variation of certain parameters influences three basic states. Finally I reproduced the diagrams that where reproduced before using a number of neuron states can be realized with transistor level simulations of the emulation.

During all my work here I neglected the synaptic term, this will be the task of my bachelor thesis: working with the input coming from the synaptic array and showing the results and deviations from ideal behaviour. I will start from ideal transistor-level simulations and carry on to analytical work, scans of temperature, monte carlo simulations including transistor missmatch and various other analysis of this term.

[2]Operational Transconductance Amplifier

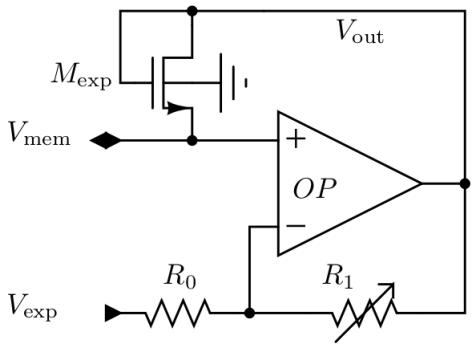


Figure 11: Schematics of the exponential term. Taken from [3]

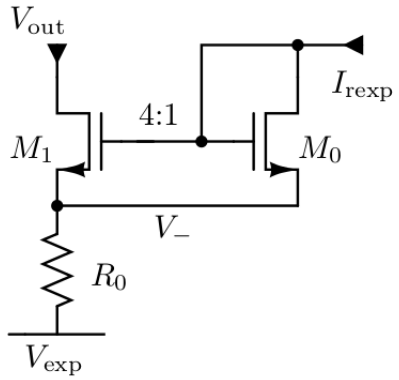


Figure 12: The current mirror emulating a adjustable resistor. Taken from [3]

6 Appendix

6.1 Analytical work on the exponential term

All credit for these calculations goes to Andreas Hartel. They depend on ideal behaviour of the OP[3]. The schematics used for these calculations are taken out of [3].

The transistor M_{exp} is connected like a diode (figure 11):

$$I_{DS} = I_0 exp\left(\frac{V_{GS} - V_{th}}{nU_T}\right)$$

The operational amplifier keeps its two terminals at the same voltage, due to negative feedback. It holds:

[3]Operational Amplifier

$$V_{mem} - V_{exp} = (V_{out} - V_{exp}) \frac{R_2}{R_1 + R_2}$$

$$\Rightarrow V_{out} = (V_{mem} - V_{exp}) \frac{R_1 + R_2}{R_2} + V_{exp}$$

For M_{exp} you get out of this:

$$\Rightarrow V_{GS,M0} = \frac{R_1}{R_2}(V_{mem} - V_{exp})$$

R_1 is realized as a variable resistor via a current mirror, channel length modulation used for mimicking of the resistive property.

$$V_- - V_{exp} = R_2 I_2 = R_2 I_{rexp}(1 + 4 + 4\lambda(V_{out} - V_-))$$

$$\Rightarrow V_{out} - V_- = \left(\frac{V_{mem} - V_{exp} - 5R_2 I_{rexp}}{R_2 I_{rexp} 4\lambda} \right) = V_{GS}$$

By this a expression for the exponential term follows:

$$I_{exp} = I_0 exp \left(\frac{V_m em - V_{exp} - 5R_2 I_{rexp}}{R_2 I_{rexp 4\lambda n U_T}} - \frac{U_{th}}{nU_T} \right)$$

This expression is used above to describe the ideal circuit behaviour of the AdEx emulation.

6.2 Documenting variables in neuron model

As a convention I choose to call the complete neuron schematic [4] "neuron model" and the with exterior circuitry realized testbench "neuron testbench". The neuron schematic contains the emulating circuit for AdEx neuron model as it is integrated in the wafer system and the testbench is build to make experiments on the bench possible. This documentation will map each variable found on the neuron model (on the schematics level) to a variable on the testbench. Further it will describe the function of all variables in the model (which term is affected, which parameter tuned) and the meaning on a circuit level approach (what kind of signal is needed, what kind of electronic component is controlled). To describe the variables I start with every term of the model on a single OTA level and describe the effect of tunable parameters on the terms. For this description I keep close to [3], but also include the names found in the schematics. The schemiatics for all terms can be found in [3].

There are two identical neurons drawn in one neuron schematics. These share the same parameters on the testbench and are identical except for the INOUT EXT term and the OUT term, where the neurons can be selected separately for interaction with other neurons.

[4] with schematic a electronic schematic realized in the *virtuoso* software is denoted

6.2.1 Leakage Term

The first term I want to describe is the leakage term in (1): "$g_l(V - E_l)$". This term is directly modelled by an OTA with negative feedback, as the OTA's ideal behaviour is described by $I_{\mathrm{OTA}} = h(V_{\mathrm{input1}} - V_{\mathrm{input2}})$ [7]. The circuit can be found in [3, figure 3.5] and has 3 pins:

- *membrane*: the circuits current output is set onto this pin. It is connected directly to the membrane potential and gives the negative feedback to the OTA.
- I_{gl}: this input current adjusts the value for g_{l} in the leakage term according to $g_{\mathrm{l}} = hI_{\mathrm{gl}}$, where h is a function of process, temperature and differential voltage [7]. Technically it is a bias current to the OTA. There are strong limits to the vaidity of the mentioned linear relation, these are discussed in [3, section 3.3.3]. I_{gl} is supplied by a current source on the neuron testbench to the neuron model and can be set as a parameter of the simulation. In the neuron model it is transferred over a current mirror (default: 3:1; fast: 1:1; slow: 27:1) onto the input pin of the circuit representation of the term described above.
- E_{l}: this input voltage is provided to the neuron model directly by a voltage source on the neuron testbench and represents the leakage reversal potential in the model. E_{l} can be set directly in the simulation. This variable is used more than one time, as explained below

6.2.2 Membrane

The Membrane is not found in the neuron model. It is set up on the neuron testbench and connected to an external pin to the neuron model (see figure 13). This model has 4 parameters, each of them can be set directly in the simulation.

- *cmem*: this is the membrane capacitance
- *cext*: an external capacitance connected in parallel to *cmem*
- E_{load}: this is a reversal potential charging the membrane over R_{load}
- R_{load}: a usually very large resistance over which *cmem* is charged by E_{load}

6.2.3 Adaptation

The adapation term represents the adaptation current in 6 and the subthreashold adaptation in 8. This circuit has 7 pins whose function is described in the following list. Important to mention is that inside this schematic the voltage V_ω is measured over the storage capacitor C_ω. V_ω is the storage variable for the amount of adaptation taking place and important later for describing the state of the neuron.

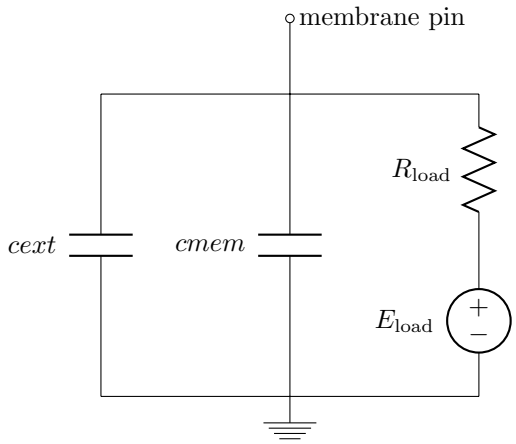


Figure 13: This circuit emulates the neuron capacitance. It is not included in the neuron model but realizied as drawn here on the neuron test bench and connected to the membrane pin.

- I_{leak}: bias current for OTA a. With this variable it is possible to control the subthreashold adaptation conductance a. This variable is mirrored to the outside (default: 3:1; fast: 1:1; slow: 27:1) of the neuron model named "$I_{gladapt}$" and can be set on the neuron testbench under this name.
- E_{leak}: the leakage reversal potential. This is the same parameter as in the leakage term and is available as pin of the neuron model. It can be set on the neuron testbench. The fact that it is the same potential as in the leakage term limits the configurability of the circuit [3, section 3.5.2].
- I_{radapt}: bias current for OTA g_w. With this variable it is possible to control the conductance g_w, which emulates the change of V_w. This variable is accessible over a current mirror (default: 32:1; fast: 8:1; slow: 640:1) as a pin on the neuron model and can be set directly on the neuron testbench.
- I_{fireb}: controls the current I_{fire}. Higher current means a higher adaptation per spike (larger change in V_ω). This current is directly mirrored onto the capacitor, as long as the digital fire signal arrives. To the on the neuron model this variable is mirrored (1:10.4) under the same name, but in the neuron testbench it is called Iadaptb.
- $fire_{\text{b}}$: triggers firing current onto capacitor when 0. The length of this signal represents t_{fire}. This is connected to the $I_{firebottom}$ and $I_{firetop}$ pins of the "Out" module, see below.
- $reset$: resets V_w to the value of the membrane capacitance. On the neuron testbench this happens every 2 seconds. Neither height nor frequency of the signal are available as parameters in the simulation.

- V_{mem}: connection to membrane

6.2.4 Synaptic Term

This circuit simulates the synaptic input terms $g_e(t)(V - E_e)$ and $g_i(t)(V - E_i)$ one at a time. The conductances control the time dependence of the circuit and are triggered by synaptic input. This synaptic input comes in very short pulses, the circuit modulates a time-dependence onto the signal (exponential decay by leaky integrator). This means two identical circuits are available for both excitatory and inhibitory input. The variable names are distinguished by the postfix "x" for excitatory and "i" for inhibitory. There are 7 pins apart from the voltage supply connected to this circuit.

- E_{syn}: sets the reversal potential for the synapse. Accessible on the neuron model via "Esyn + i/x" and can be set under this name on the testbench.
- V_{syn}: voltage offset for integrator circuit. Accessible on the neuron model via "Vsyn + i/x" and can be set under this name on the testbench.
- V_{syntc}: sets resistance for leaky integrator via the circuit described in [3, section 3.6.2]. The resistance does not depend linearly on this voltage, exact measurements can be found in the cited Dissertation. Accessible on the neuron model via "Vsyntc + i/x" and can be set under this name on the testbench.
- I_{intbb}: offset current for differential pair in operational amplifier, can be used to tune the differential gain. It is accessible on the neuron model via a current mirror (1:1) under the name "Iintbb + i/x" and can be set in the simulation.
- *membrane*: connected to membrane potential, gives negative feedback.
- I_{conv}: sets the influence of the synaptic term, higher values mean higher influence of the synaptic term. Technically this a bias current to an OTA whose output current is proportional to an exponential decay modelled by an leaky integrator. This output current is an bias current again to an OTA whose current is proportional to the difference between reversal potential and membrane potential. This variable is available on the neuron model via "Iconv + i/x" and can be set under this name on the testbench.
- I_{syn}: The synaptic input current usually coming from the synapse array. This current can be controlled directly at a pin on the neuron model under the name "Isyn + i/x" and can be set in the simulation to constant values.

6.2.5 Exponential Term

The exponential term drives the membrane potential to the spiking threshold as soon as a certain spiking threshold is reached, described by $I_{\text{exp}} = -g_l \Delta_t exp\left(\frac{V-V_t}{\Delta_t}\right)$.

The term is emulated by the circuit seen in [3, Figure 3.22]. The exponential dependency is realized by a mosfet connected like a diode. The rest of the circuit should control the current through that diode. The exact description can be found in [3, section 3.7], here we only describe the 5 controllable pins and their meaning

- I_{rexp}: Technically this current is mirrored by a current mirror (3:1), which realizes a adjustable resistor. Higher current results in lower resistance. The effect of this lower resistance is a higher Δ_t and therefore lower exponential threshold. This value is accessible as pin on the neuron model and accessible on the neuron testbench
- I_{bexpb}: This current is the offset current for the operational amplifier in the circuit. A higher value of this current results in a stronger amplification of differences at the Inputs of the amplifier. It is mirrored to the outside of the neuron model (1:2) and accessible under the same name on the neuron testbench
- V_{exp}: sets the voltage at which the exponential term starts influencing the membrane. Higher values result in a higher threshold, but this voltage is not identical to the threshold voltage as it is transformed according to [3, section3.7.1]
- V_{bexpb}: turns a buffer for the exponential voltage on and off (high value: off, low value on), if the buffer is off V_{exp} is replaced by a high impedance. This pin is available on the neuron schematics and connected to vbb on the outside, permanently it is on a voltage around 1.2 V
- *membrane*: connected directly to the membrane

6.2.6 Spike Detection

The spike detection circuit compares the spike threshold with the current membrane voltage. It is connected to various pins but not important in this internship, so we decide to not describe the individual pins, but only list them.

- *Ispikeamp*: offset voltage for the amplifier comparing the threshold voltage with the membrane voltage. Accessible directly as pin on the neuron model and can be set in the neuron testbench
- *membranetop*: connected to the membrane at the top, when the membranes are to be connected. There is an analogous *membranebottom* pin. This pin is accessible on the neuron model and connected to nothing on the neuron testbench
- *conncettotopb*: this variable controls the connection to the upper membrane. If the value of *conncettotopb* or *memi5* is 0 the neuron membrane is connected to the top neuron. *conncettotopb* is hard-wired to vdd (1) on the neuron testbench. There is an analogous *connecttobottomb* pin, which is connected to nothing on the neuron testbench

- *fireouttop*: Inverted fire signal of this neuron.
- *fireintop*: Signal coming from next neuron, gets inverted and is set on the fire pin.
- *memi*: these variables are responsible for the connection to other neurons, they are all connected to voltage sources on the neuron testbench. They can take the digital values 0 and 1 (0 and 1.8 V respectively). For every memi pin there is a memib pin, that gives out the inversion of the signal. Inside the connection block the value of these pins is written to SRAM cells with a certain writing frequency given by the pulsed *writeMem*. Each of them is accessible as a output pin of the neuron model and can be assigned their digital values in the neuron testbench
  - *memi0, memi1 and memi2* are translated to ext0, ext1 and ext2 over the SRAM cells and given to the outside via an ext pin.
  - *memi3*: This pin connects the two membranes realized on the neuron testbench: if the digital value is 1, the membranes are connected to each other. It is accessible as *connect12* on the neuron testbench and usually set to 1.
  - *memi4*: controls an inverter connected to the output of the comparator that detects the spike. If memi4 is set to 1, the output is inverted and connected to the next stages fire, fireouttop, post), if it is set to 0 the spike signal never reaches these stages. Its name on the neuron testbench is *neuron2active*. The pin *memi7* is analogous to this pin and controlled via *neuron1active* on the neuron testbench.
  - *memi5*: set as connectTop on neuron testbench, controlls inverter for *firein* signals. *memi6*, set as connectBottom on the testbench controlls the same for the below neuron.
- *reset:* Resets the output of the comparator circuit onto ground.
- *ext*: connected to the INOUT EXT term. No function in this circuit.
- *writeMem*: Controlls the wordline of SRAM cells that store the values for *memi*, running with 10 Mhz on neuron testbench.
- *Vt*: Spiking threshold, compared by the comparator with the membrane voltage.

6.2.7 Reset

As soon as a spike is detected by the spike detection circuit the reset mechanism pulls the membrane voltage to the reset value. It is controlled by 5 pins.

- $fire$: digital fire signal put out by the Spikedetection term.
- *membrane*: connected to membrane.

- $V_{iresetgolbal}$: Enables the reset mechanism when "high". On the neuron testbench its hardwired to be a voltage close to the positive rail, as the reset is always enabled.

- V_{reset}: Voltage on which the membrane voltage is reset when the spike detection finds that the threshold voltage is reached.

- i_{pulse}: recharges a capacitor that closes the reset. This capacitor is charged in the standard case, but uncharged when a fire signal arrives at the reset term. When the current is higher, the reset voltage is presented to the neuron for a longer time.

6.2.8 INOUT EXT

To perform experiments like they are possible with real neurons, this term opens the possibility to connect the neuron to the outside or inject currents onto the membrane. As there are two neurons available, there is a possibility to select one of them as an output and on which to inject a current

- $current_{in}$: If the $current_{enable}$ signal for the respective neuron is on (table 4) the input current is set on the membrane. This value can be set directly on the neuron testbench.

- *out*: output of the INOUT EXT term, connection to membrane is made possible via a buffer circuit that can be controlled by the ext variables described below. If the buffer is disabled the output is set to high impedance. This pin is accessible on the neuron model and connected to nothing on the testbench

- *ext0, ext1, ext2*: the ext pins are connected over the OUT module described above, they are accessible under the same names on the neuron testbench and carried into the neuron schematics as memi0, memi1 and memi 2. They can take binary values.

To descibe the behaviour due to the ext variables we analyse the circuits and transform it to truth tables:

Connection of the membrane to the *out* pin is realized by the buffer mentioned above, the following truth tables show in which way the buffers can be controlled for neuron 0 and 1:

The $current_{in}$ connection is controlled by just two variables: ext1 and ext2. These control logic gates that enable or disable a switch allowing the current to flow on the membrane.

ext2	ext1	ext0	$\text{buffer}_{\text{enable}}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

(a) neuron 0: $\text{buffer}_{\text{enable}} = \overline{ext1 \cdot ext2} \cdot ext0$

ext2	ext1	ext0	$\text{buffer}_{\text{enable}}$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(b) neuron 1: $\text{buffer}_{\text{enable}} = \overline{ext0 \cdot ext2} \cdot ext1$

Table 3: these tables describe the control of the output circuit by the variables ext0, ext1 and ext2.

ext2	ext1	$\text{current}_{\text{enable}}$
0	0	0
0	1	0
1	0	0
1	1	1

(a) neuron 0: $\text{current}_{\text{enable}} = ext1 \cdot ext2$

ext2	ext1	$\text{current}_{\text{enable}}$
0	0	0
0	1	0
1	0	1
1	1	0

(b) neuron 1: $\text{current}_{\text{enable}} = \overline{ext1} \cdot ext2$

Table 4: the way in which the variables ext1 and ext2 control the current onto the membrane

ext2	ext1	ext0	$\text{buffer}_{\text{enable}}0$	$\text{buffer}_{\text{enable}}1$	$\text{current}_{\text{enable}}0$	$\text{current}_{\text{enable}}1$
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	1	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	0	1	0

Table 5: summary table concluding the above derivations

7 References

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